IN THE CLAIMS:

Listing of claims:

1. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.6 V is used,

a thickness of the SOI film is 0.084 μm or greater and 0.094 μm or smaller, and an impurity concentration of the SOI film is $7.95 \times 10^{17}/cm^3$ or greater and $8.05 \times 10^{17}/cm^3$ or smaller.

2. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.6 V is used,

a thickness of the SOI film is 0.089 μm or greater and 0.099 μm or smaller, and an impurity concentration of the SOI film is $8.95 \times 10^{17}/cm^3$ or greater and $9.05 \times 10^{17}/cm^3$ or smaller.

3. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.6 V is used,

a thickness of the SOI film is 0.093 μm or greater and 0.103 μm or smaller, and an impurity concentration of the SOI film is $0.095 \times 10^{18}/cm^3$ or greater and $1.005 \times 10^{18}/cm^3$ or smaller.

4. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.6 V is used,

a thickness of the SOI film is 0.096 μm or greater and 0.106 μm or smaller, and an impurity concentration of the SOI film is $1.095 \times 10^{18}/ cm^3$ or greater and $1.105 \times 10^{18}/cm^3$ or smaller.

5. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.6 V is used,

a thickness of the SOI film is 0.100 μm or greater and 0.110 μm or smaller, and an impurity concentration of the SOI film is $1.195 \times 10^{18}/cm^3$ or greater and $1.205 \times 10^{18}/cm^3$ or smaller.

6. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.8 V is used,

a thickness of the SOI film is 0.068 μm or greater and 0.078 μm or smaller, and an impurity concentration of the SOI film is $7.95 \times 10^{17}/cm^3$ or greater and $8.05 \times 10^{17}/cm^3$ or smaller.

7. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.8 V is used,

a thickness of the SOI film is 0.074 μm or greater and 0.084 μm or smaller, and an impurity concentration of the SOI film is $8.95 \times 10^{17}/cm^3$ or greater and $9.05 \times 10^{17}/cm^3$ or smaller.

8. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.8 V is used,

a thickness of the SOI film is 0.078 μm or greater and 0.088 μm or smaller, and an impurity concentration of the SOI film is $0.095 \times 10^{18}/cm^3$ or greater and $1.005 \times 10^{18}/cm^3$ or smaller.

9. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.8 V is used,

a thickness of the SOI film is 0.083 μm or greater and 0.093 μm or smaller, and an impurity concentration of the SOI film is $1.095 \times 10^{18}/cm^3$ or greater and $1.105 \times 10^{18}/cm^3$ or smaller.

10. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.8 V is used,

a thickness of the SOI film is 0.087 μm or greater and 0.097 μm or smaller, and an impurity concentration of the SOI film is $1.195 \times 10^{18}/cm^3$ or greater and $1.205 \times 10^{18}/cm^3$ or smaller.

11. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 1.0 V is used,

a thickness of the SOI film is 0.057 μm or greater and 0.067 μm or smaller, and an impurity concentration of the SOI film is $7.95 \times 10^{17}/cm^3$ or greater and $8.05 \times 10^{17}/cm^3$ or smaller.

12. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 1.0 V is used,

a thickness of the SOI film is 0.063 μm or greater and 0.073 μm or smaller, and an impurity concentration of the SOI film is $8.95 \times 10^{17}/cm^3$ or greater and $9.05 \times 10^{17}/cm^3$ or smaller.

13. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 1.0 V is used,

a thickness of the SOI film is 0.068 μm or greater and 0.078 μm or smaller, and an impurity concentration of the SOI film is $0.095 \times 10^{18}/cm^3$ or greater and $1.005 \times 10^{18}/cm^3$ or smaller.

14. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 1.0 V is used,

a thickness of the SOI film is 0.072 μm or greater and 0.082 μm or smaller, and an impurity concentration of the SOI film is $1.095 \times 10^{18}/cm^3$ or greater and $1.105 \times 10^{18}/cm^3$ or smaller.

15. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 1.0 V is used,

a thickness of the SOI film is 0.076 μm or greater and 0.086 μm or smaller, and an impurity concentration of the SOI film is $1.195 \times 10^{18}/cm^3$ or greater and $1.205 \times 10^{18}/cm^3$ or smaller.

16. (currently amended) A semiconductor device as in claim 1, further comprising first and second low concentration diffusion regions in contact with source/drain regions, the first and second low concentration diffusion regions having a lower impurity concentration than the source/drain regions, the first and second low concentration diffusion regions being separated from each other by a portion of the SOI film under the gate dielectric film, wherein a portion of each of the low concentration diffusion regions extends under the gate electrode.

17. (new) A semiconductor device as in claim 6, further comprising first and second low concentration diffusion regions in contact with source/drain regions, the first and second low concentration diffusion regions having a lower impurity concentration than the source/drain regions, the first and second low concentration diffusion regions being separated from each other

by a portion of the SOI film under the gate dielectric film, wherein a portion of each of the low concentration diffusion regions extends under the gate electrode.

18. (new) A semiconductor device as in claim 11, further comprising first and second low concentration diffusion regions in contact with source/drain regions, the first and second low concentration diffusion regions having a lower impurity concentration than the source/drain regions, the first and second low concentration diffusion regions being separated from each other by a portion of the SOI film under the gate dielectric film, wherein a portion of each of the low concentration diffusion regions extends under the gate electrode.